



The diagram, labeled FIG. 2, is a timing diagram titled "Clock Freeze Timing Diagram". It shows the relationship between several signals over time, marked by vertical grid lines and time points T0, T1, T2, and T3. The signals are:

- System Clock 205:** A periodic square wave signal.
- Clock Freeze Event 210:** A signal that transitions from low to high at time T1 and remains high.
- Qualified Clock Freeze 215:** A signal that transitions from low to high at time T3 and remains high.
- CSL Clock 220:** A periodic square wave signal that continues after T3.
- DMA Request 225:** A signal that is low throughout the entire duration.
- DMA Grant 230:** A signal that is high from T0 to T1 and then transitions to low at T1, remaining low thereafter.

Time points T0, T1, T2, and T3 are marked on the horizontal axis. T3 is specifically identified by an upward-pointing arrow and the text "Last Pending Transaction Completed". A reference numeral 200 points to the top right corner of the diagram area.

FIG. 2